A Method For Generating Optimized Constraint Systems For Retimable Digital Designs

ABSTRACT

A method for generating timing constraint systems, where the constrained object is a digital circuit., is provided, where the constraints are generated for the use of a digital logic optimization (synthesis) tool. The synthesis tool is used to optimize the circuit, under the applied constraints, so that the circuit exhibits certain desirable timing properties, while at the same time minimizing hardware cost and various other properties. The particular class of timing constraints generated by the disclosed invention is useful when the circuit is to be retimed after optimization. Typically, the joint use of the described invention and retiming results in improvements in the overall cost/performance tradeoff curve of the design. The invention comprises a method that comprises the following steps: (1) the flip-flops of the design are replaced with buffers having a negative delay whose magnitude is approximately the desired clock cycle time of the design; and (2) cycles in the design are broken using flip-flops having an infinite or quasi-infinite clock frequency. Following optimization by the synthesis tool, the temporary changes can be reverted, and retiming performed on the circuit.